

221	Subclass
ISSUE CLASSIFICATION	

PATENT NUMBER

## U.S. REISSUE PATENT APPLICATION

<b>DB</b> <b>O.I.P.E.</b> SCANNED <u>TRC</u> Q.A. <u>AN</u>	<b>O.G. PUBLICATION DATE</b> <u>5-5-51</u>	<b>REISSUE PATENT DATE</b>
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APPLICATION NO. 09/328910	CONT/PRIOR D F	CLASS 257	SUBCLASS	ART UNIT 2811	EXAMINER J. Lee R
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LEADFRAME SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE USING THE SAME  
AND METHOD OF AND PROCESS FOR FABRICATING THE TWO

PTO-2040  
12/99

☐ SURRENDER OF ORIGINAL PATENT

**Ex. 1011**

**PREPARED AND APPROVED FOR ISSUE**

# ISSUING CLASSIFICATION

[illegible]

<input checked="" type="checkbox"/> <b>TERMINAL DISCOUNT</b>	<b>DRAWINGS</b> Sheet Drawing _____ Fig. Drawing _____ Photo _____ 21 35 24, 25			<b>CLAIMS ALLOWED</b> Total Claims _____ 59		Print Claim for O.G. _____ 1	
	<input checked="" type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.			<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of Pat. No. _____.		<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The terminal _____ months this patent have been disclaimed.			_____ (Assistant Examiner) _____ (Date)		<b>ISSUE FEE</b>		Amount Due _____
<b>FINAL SPRE REVIEW</b>			_____ (Legal Instruments Examiner) _____ (Date)		Date Paid _____		<b>ISSUE BATCH NUMBER</b>

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